IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) An apparatus comprising:

a processor;

an expander memory bridge location, the expander memory bridge location including a location to couple to and allow installation of an expander memory bridge;

a memory coupled to the expander memory bridge location; and

a controller coupling the processor to the expander memory bridge location, the controller including intercept logic to intercept and block communication from the processor to the expander memory bridge location and to emulate an expander memory bridge including responding to the processor regardless of whether the expander memory bridge is or is not installed at the location.

2. (Original) The apparatus of claim 1, wherein the controller includes a disable intercept logic bit.

3. (Original) The apparatus of claim 2, wherein the memory includes a mirror configuration.

4. (Original) The apparatus of claim 2, wherein the memory includes a redundant array of independent memories.

5. (Original) The apparatus of claim 3, wherein the processor includes a complex instruction set processor.

6. (Original) The apparatus of claim 1, wherein the bus controller includes an expander memory bridge plugged-in bit.

7. (Original) The apparatus of claim 6, wherein the memory includes a double data rate memory.

8. (Original) The apparatus of claim 1, further comprising an operating system to operate in cooperation with the processor, the operating system free of support for hot-pluggable components.

9. (Canceled)

10. (Previously Presented) A method comprising:

intercepting and blocking a status request to a device, regardless of whether the device is installed, wherein intercepting and blocking the status request to the device, regardless of whether the device is installed, includes intercepting and blocking the status request during a configuration access to the device; and

responding to the status request.

11. (Original) The method of claim 10, wherein responding to the status request includes emulating a response the device returns when the status request is not blocked.

12. (Original) The method of claim 11, wherein emulating a response the device returns when the status request is not blocked includes emulating the response of a memory bridge.

13. (Previously Presented) A method comprising:

intercepting and blocking a status request to a device, regardless of whether the device is installed; and

responding to the status request, wherein responding to the status request includes responding that the device is available when the device is not installed.

14. (Original) The method of claim 13, wherein responding to the status request includes responding to the status request in a time period substantially equivalent to the time period in which a non-intercepted status request is responded to.

15. (Original) The method of claim 14, wherein intercepting and blocking the status request to the device, regardless of whether the device is installed, includes intercepting the status request directed to configuration space.

16. (Original) The method of claim 9, further comprising, removing the device, if the device is installed.

17. (Original) The method of claim 16, wherein removing the device, if the device is installed, includes removing a memory device.

18. (Original) The method of claim 9, further comprising, adding the device, if the device is not installed.

19. (Original) The method of claim 18, wherein adding the device if the device is not installed, includes adding a double data rate memory device.

20. (Previously Presented) A method comprising:

intercepting and blocking communications from a processor to an expander memory bridge;

emulating the expander memory bridge including responding to the processor regardless of whether the expander memory bridge is or is not installed at the location; and

setting a disable intercept bit to stop interception and blocking of communications from the processor to the expander memory bridge.

21. (Original) The method of claim 20, further comprising configuring the expander memory bridge.

22. (Original) The method of claim 21, further comprising resetting the disable intercept bit.

23-25. (Canceled)

26. (Previously Presented) A system comprising:

a processor;

an expander memory bridge location;

a memory coupled to the expander memory bridge location;

a controller including intercept logic to intercept and block communication from the processor to the expander memory bridge location and to emulate an expander memory bridge including responding to the processor regardless of whether the expander memory bridge is or is not installed at the location;

a display coupled to the processor; and

a storage device coupled to the processor.

27. (Original) The system of claim 26, wherein the display comprises a plasma display.

28. (Original) The system of claim 26, wherein the storage device comprises a magnetic storage device.